REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-28 are in this case. Claims 1-28 have been rejected under § 102(b). Claims 6, 17, 22 and 28 have been rejected under § 103(a). Claims 10 and 11 have been objected to. Dependent claims 24 and 25 have been canceled. Independent claim 1, 7, 18, 23 and 26 and dependent claims 3, 4, 9, 10, 12, 14, 15, 19-21 and 27 have been amended.

The claims before the Examiner are directed toward methods of assembling and testing electronic devices, specifically, systems-in-package (SIPs), and to a device so assembled and tested. A CPU, a nonvolatile memory and a volatile memory are fabricated on respective, physically independent chips and are packaged together in a common package with the CPU operationally connected to the memories. Testing programs for the memories are stored in the nonvolatile memory and are executed by the CPU from the volatile memory to test the memories. Then the CPU is tested.

§ 102(b) Rejections – Chesley '142

The Examiner has rejected claims 1-28 under § 102(b) as being anticipated by Chesley, US Patent No. 4,333,142 (henceforth, "Chesley '142"). The Examiner's rejection is respectfully traversed.

Chesley '142 teaches a computer fabricated on a single wafer **11** with redundant components and configured to test itself when power is applied to identify and not use inoperative components. Specifically, the computer includes many CPU chips **12**, many ROM chips **13** and many RAM chips **14**. When power is applied to the computer, each CPU tests itself until a working CPU is found. The working CPU

does checksum testing of the ROMs until a working ROM is found. The working CPU then runs a test routine stored in the working ROM to test the RAMs in order to identify working RAMs.

Conceptually, the difference between the present invention and the teachings of Chesley '142 is that the teachings of Chesley '142 are directed at the operation of a computer whereas the present invention is methods of assembly of an electronic device, specifically of a SIP. To ore clearly distinguish the present invention from the teachings of Chesley '142, independent method claims 1, 7, 18 and 26 have been amended to recite methods, of assembling and testing an electronic device such as a SIP, that include the steps of fabricating the components recited in these claims (a CPU and at least one memory in the case of claim 1; a CPU, a nonvolatile memory and a volatile memory in the case of claim 7; a CPU and a nonvolatile memory in the case of claim 18; a nonvolatile memory and a volatile memory in the case of claim 26) on respective, physically independent chips, and packaging the components within a common package with the components operationally connected to each other. Independent device claim 23 has been amended similarly by including in claim 23 the limitations of claims 24 and 25 and adding the limitation that the nonvolatile memory, the volatile memory and the CPU are fabricated on respective, physically independent chips. This is in contrast to the chips of Chesley '142 that are all fabricated on the same wafer **11** and so are never physically independent. Correspondingly, dependent claims 24 and 25 have been canceled and the steps of dependent claims 3, 4, 9, 10, 14, 19-21 and 27 have been relabeled.

With regard to the support of these amendments, all the limitations now added to the independent claims are found in claims 23-25 as filed, except for the fabrication of the various components on physically independent chips. The limitation that the

various components are fabricated on physically independent chips is inherent in the description of the prior art of assembling SIPs on page 1 lines 13-23 of the specification:

> The advent of integrated circuits made it possible to fabricate an entire electronic circuit in a single package. Traditionally, such chips were packaged in separate packages, which then were connected together, for example after being mounted together on printed circuit boards, to form complete systems. More recently, in order to reduce the size of electronic systems further, some manufacturers have begun to package several chips, related to several technologies, in the same package. For example, a processor for controlling a cellular telephone could include a central processing unit (CPU), a nonvolatile memory such as a flash memory and a volatile memory such as a SDRAM, each fabricated on its own chip, and all packaged in the same package. Such a system is called a "System-in-Package" (SIP), a "MultiChip Package" (MCP) or a "MultiChip Module" (MCM). (emphasis added)

If the chips were packaged together in separate packages before being connected together, then the chips were inherently physically independent of each other. In a SIP, these initially physically independent chips are operationally connected and packaged together in a common package. The present invention adds to this prior art assembly process an innovative method of testing the chips that are thus assembled.

Thus, the present invention, as recited in independent claims 1, 7, 18, 23 and 26 as now amended, is not anticipated by Chesley '142. Furthermore, the present invention, as recited in independent claims 1, 7, 18, 23 and 26 as now amended, is not even obvious from Chesley '142. As noted above, the teachings of Chesley '142 are directed at the operation of a computer, not at the assembly of an electronic device. One ordinarily skilled in the art would not apply the teachings of Chesley '142 to testing the components of and electronic device in the context of assembling the device.

With independent claims 1, 7, 18 and 26 allowable in their present form it follows that claims 2-6, 8-17, 19-22, 27 and 28 that depend therefrom also are allowable.

§ 103(a) Rejections – Chesley '142 in view of Takizawa '663

The Examiner has rejected claims 6, 17, 22 and 28 under § 103(a) as being unpatentable over Chesley '142 in view of Takizawa, US Patent No. 6,198, 663. The Examiner's rejection is respectfully traversed.

It is demonstrated above that independent claims 1, 7, 18 and 26 are allowable in their present form. It follows that claims 6, 17, 22 and 28 that depend therefrom also are allowable.

Objections

The Examiner has objected to claims 10 and 11 because of the complicated language of claim 10. The language of claim 10 now has been simplified without adding new matter to the claim.

Applicant appreciates the Examiner's proposed rewording of claim 10, but the Examiner's proposed rewording changes the second clause of claim 10 to "said loading of the testing program into the volatile memory from the nonvolatile memory", which lacks a verb. Applicant believes that applicant's rewording of this clause to "so that said loading of the testing program into the volatile memory is from the nonvolatile memory" simplifies the wording of claim 10 while preserving grammatical correctness.

Amendments to the Specification

An inadvertent typographical error on page 2 line 7 has been corrected. Applicant thanks the Examiner for pointing out this error.

No new matter has been added.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1, 7, 18, 23 and 26, and hence dependent claims 2-6, 8-17, 19-22, 27 and 28 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

Mark M. Friedman
Attorney for Applicant
Registration No. 33,883

Date: April 30, 2006